SPECIFICATION

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[METHOD FOR FABRICATING MASK ROM WITH SELF-ALIGNED CODING]

Background of Invention

[0001] Field of Invention

[0002]] The present invention relates to a method for fabricating a read-only memory (ROM). More particularly, the present invention relates to a method for fabricating a mask read-only memory (Mask ROM).

[0003] Description of Related Art

[0004] Read-only memory (ROM) is non-volatile and can retain data as disconnected from power supply. Therefore, various electronic products use ROM to store data needed for their operations. In the family of ROM, the simplest one is namely the Mask ROM, which uses MOS transistors as memory cells and is programmed by implanting ions into the channels of selected memory cells to change the threshold voltages thereof. The presence of implanted ions determines the conducting state (On/Off) of a memory cell during reading operation.

[0005] A Mask ROM comprises a plurality of buried bit lines in a substrate and a plurality of polysilicon word lines on the substrate crossing over the buried bit lines, while the substrate under the word lines and between the buried bit lines serve as the channels of the memory cells. The process of implanting ions into the channels of selected memory cells is called coding implantation, and the data (0 or 1) stored in each memory cell is dependent on the presence of implanted ions.

[0006] Refer to FIG. 1~2, wherein FIG. 1 illustrates a top view of a Mask ROM in the prior

art, and FIG. 2 illustrates a cross-sectional view of the Mask ROM along line I-I. The Mask ROM comprises a substrate 100, parallel buried bit lines 104 and parallel word lines 102 crossing over the buried bit lines 104, wherein the word lines 102 are isolated from the substrate 100 by a gate oxide layer 108. The Mask ROM is programmed by implanting ions into the channels of selected memory cells, such as the channel of the memory cell under a coding window 106, to change the threshold voltages thereof. The presence of implanted ions determines the conducting state (On/Off) of a memory cell during reading operation.

[0007] Refer to FIG. 2 again, a patterned photoresist layer 110 is formed with a coding window 106 by using a lithography process. A coding implantation 112 is performed to implant ions into the substrate 100 under the word line 102 exposed by the coding window 106, so as to program the Mask ROM.

[0008] As the Mask ROM cell is miniaturized to increase the integration of the Mask ROM device, a photo-mask with small aperture sizes is required to form small coding windows, otherwise coding errors may occur because of the misalignment between larger coding windows and selected channel regions. However, fabricating a photo-mask with small aperture sizes is time-consuming, and is more difficult and more expensive.

[0009] Moreover, since the corners of the coding windows are rounded because of light scattering, coding errors easily occur in the prior art.

Summary of Invention

[0010] Accordingly, this invention provides a method for fabricating a Mask ROM with self-aligned coding without using a photo-mask with small aperture sizes, so as to reduce the fabrication cost of the photo-mask.

[0011] This invention also provides a method for fabricating a Mask ROM to prevent coding errors caused by deformation (corner rounding) of the coding windows, so as to improve the programming accuracy.

[0012]

A method for fabricating a Mask ROM with self-aligned coding of this invention comprises the following steps. A plurality of buried bit lines are formed in a substrate,

and then a conductive layer and a first blocking layer are sequentially formed on the substrate. The first blocking layer and the conductive layer are patterned into a plurality of first blocking strips and a plurality of word lines, respectively, and then a plurality of second blocking strips are formed between the word lines and between the first blocking strips. Thereafter, a first photoresist pattern is formed over the substrate, and then the first blocking strips are patterned into an array of blocking bumps, which define a plurality of pre-coding windows with the second blocking strips. After the first photoresist pattern is removed, a coding photoresist layer is formed on the substrate with a plurality of coding windows exposing selected pre-coding windows, wherein a coding widow is larger than a pre-coding window. Then, a coding implantation is performed using the coding photoresist layer, the blocking bumps and the second blocking strips as a mask to form implanted coding regions in the substrate under the pre-coding windows exposed by the coding windows. The coding photoresist layer is then removed.

[0013] Since the blocking bumps and the second blocking strips together define the pre-coding windows and block the regions outside the coding regions, the coding implantation can self-align to the coding regions under the coding windows to avoid coding errors even if misalignment occurs. Therefore, the coding windows can be formed larger without causing coding errors.

[0014] Moreover, each coding window is surrounded by two blocking bumps and two of the second blocking strips, and therefore has a tetragonal shape. Since the coding implantation profile of a selected memory cell under a coding window is determined by the shape of the corresponding pre-coding window, corner rounding of the coding windows will not adversely affect the coding implantation profile to cause coding errors.

[0015] Furthermore, since the coding windows can be formed larger, the aperture sizes of the photo-mask can be increased to reduce the cost of fabricating the photo-mask and to shorten the turn-around time (TAT) of mass production.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0018] FIG. 1 schematically illustrates a top view of a Mask ROM in the prior art;

[0019] FIG. 2 schematically illustrates a cross-sectional view of the Mask ROM in FIG. 1 along line I-I;

[0020] FIG. 3A~3F schematically illustrate a process flow of fabricating a Mask ROM with self-aligned coding according to a preferred embodiment of this invention in a top view;

[0021] FIG. 4A~4F illustrate the same process flow illustrated in FIG. 3A~3F in a cross-sectional view along line II-II;

[0022] FIG. 5A~5F illustrate the same process flow illustrated in FIG. 3A~3F in a cross-sectional view along line III-III; and

[0023] FIG. 6A~6F illustrate the same process flow illustrated in FIG. 3A~3F in a cross-sectional view along line IV-IV.

Detailed Description

[0024] FIG. 3A~3F, 4A~4F, 5A~5F and 6A~6F schematically illustrate a process flow of fabricating a Mask ROM with self-aligned coding according to the preferred embodiment of this invention. FIG. 3A~3F illustrate the process flow in a top view, and FIG. 4A~4F, 5A~5F and 6A~6F in three cross-sectional views along line II-II, line III-III and line IV-IV, respectively.

[0025] Refer to FIG. 3A, 4A, 5A and 6A, a substrate 200, such as a silicon substrate, is provided, and then a gate dielectric layer 202 is formed on the substrate 200. The gate dielectric layer 202 comprises, for example, silicon oxide, and is formed by using thermal oxidation.

[0026] A plurality of buried bit lines 204 are formed in the substrate 200 with the

following steps, for example. A patterned mask layer is formed exposing a plurality of strip regions of the substrate, and a doping process is performed using the patterned mask layer as a mask to dope the strip regions of the substrate. A rapid thermal annealing process (RTA) is then conducted to repair the damaged lattice structures in the substrate 200. In the above process, the doping process is, for example, an ion implantation process using an N-type ion. The patterned mask layer is then removed.

[0027] Thereafter, a conductive layer 206, an isolating layer 208 and a blocking layer 210 are sequentially formed on the substrate 200. The conductive layer 206 comprises a material such as polycide, and is formed by, for example, forming a doped polysilicon layer 212 on the substrate 200 by using chemical vapor deposition (CVD) with in-situ doping, and then forming a metal silicide layer 214 on the polysilicon layer 212. The metal silicide layer 214 comprises a material such as nickel silicide ($NiSi_x$), tungsten silicide (WSi_x), cobalt silicide ($CoSi_x$), titanium silicide ($TiSi_x$), platinum silicide ($PtSi_x$) or palladium silicide ($PdSi_x$). The isolating layer 208 comprises an isolating material such as silicon oxide to isolate the conductive layer 206 from the blocking layer 210, and is formed by using thermal oxidation or chemical vapor deposition (CVD). The blocking layer 210 comprises, for example, polysilicon, and is formed by using a method such as CVD. Besides, the blocking layer 210 may comprise silicon nitride, silicon oxynitride or other materials.

[0028] Refer to FIG. 3B, 4B, 5B and 6B, a lithography process and an etching process are performed to pattern the blocking layer 210, the isolating layer 208 and the conductive layer 206 to form a plurality of word lines 216 and a plurality of blocking strips 218. A word line 216 and the blocking strip 218 thereon together constitute a stacked strip structure 220.

[0029] Refer to FIG. 3C, 4C, 5C and 6C, another blocking layer (not shown) is formed all over the substrate 200 to fill the gaps between the stacked strip structures 220. A portion of the blocking layer is removed until the tops of the stacked strip structures 220 are exposed in order to form a plurality of blocking strips 222 between the stacked strip structures 220. The blocking strips 222 comprise a material different from that of the blocking strips 218, so that an etching selectivity can be made between them. The blocking strips 222 comprises, for example, silicon oxide formed

by using CVD with tetraethylorthosilicate (TEOS)/O_3 as reaction gases. The method for removing a portion of the blocking layer to form the blocking strips 222 comprises chemical mechanical polishing (CMP) or etching-back.

[0030] Refer to FIG. 3D, 4D, 5D and 6D, a patterned mask layer 224 is formed on the substrate 200. The mask layer 224 comprises a material such as photoresist, and consists of a plurality of strip patterns perpendicular to the stacked strip structures 220, wherein each strip pattern is located over a buried bit line 204.

[0031] Refer to FIG. 3E, 4E, 5E and 6E, an anisotropic etching process is performed to remove the blocking strips 218 exposed by the mask layer 224 to form an array of blocking bumps 226. In the anisotropic etching process, the mask layer 224 serves as an etching mask, and the isolating layer 208 serves as an etching stop layer. The mask layer 224 is then removed. The blocking bumps 226 and the blocking strips 222 together define a plurality of pre-coding windows 230 and a plurality of pre-coding regions 228 in the substrate 200 under the pre-coding windows 230.

[0032] Refer to FIG. 3F, 4F, 5F and 6F, a coding mask layer 232 with coding windows 234 and 236 therein is formed on the substrate 200 by sequentially performing photoresist coating, exposure, development and related processes, wherein the exposing process uses a coding photo-mask. Then, a coding implantation is performed using the mask layer 232, the blocking bumps 226 and the blocking strips 222 as a mask to implant ions into the substrate 200 under the pre-coding windows 230 exposed by the coding windows 234 and 236 to form implanted coding regions 238. In this step, since the pre-coding windows 230 have been formed under, the coding implantation can self-align to the selected channel regions under the coding windows 234 and 236 even if the coding window 236 is misaligned to the pre-coding regions 228. Therefore, the coding windows 234 and 236 in the coding mask layer 232 as well as the apertures on the photo-mask can be formed larger without causing coding errors. Moreover, since the implantation profile of a implanted coding regions 238 is determined by two blocking bumps 226 and two blocking strips 222, a required tetragonal implantation profiles can be obtained without being affected by corner rounding of the coding windows 234 and 236. Furthermore, since the coding windows 234 and 236 can be formed larger, the aperture sizes on the photo-mask

can be increased to reduce the cost of fabricating the photo-mask and to shorten the turn-around time (TAT) of mass production.

[0033] Thereafter, the coding mask layer 232 is removed, and subsequent processes are performed to finish the manufacturing process of the Mask ROM. Since the subsequent processes are well known to those skilled in the art, their descriptions are omitted.

[0034] As mentioned above, Since the blocking bumps and the second blocking strips together define the pre-coding windows and block the regions outside the coding regions, the coding implantation can self-align to the coding regions under the coding windows to avoid coding errors even if misalignment occurs. Therefore, the coding windows can be formed larger without causing coding errors.

[0035] Moreover, each coding window is surrounded by two blocking bumps and two of the second blocking strips, and therefore has a tetragonal shape. Since the coding implantation profile of a selected memory cell under a coding window is determined by the shape of the corresponding pre-coding window, corner rounding of the coding windows will not adversely affect the coding implantation profile to cause coding errors.

[0036] Furthermore, since the coding windows can be formed larger, the aperture sizes of the photo-mask can be increased to reduce the cost of fabricating the photo-mask and to shorten the turn-around time (TAT) of mass production.

[0037] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.